In The Claims

Please cancel claims 1-47 without prejudice, and add new claims 48-69.

Claims 1-47 (canceled).

48. (new) A gated semiconductor assembly, comprising:

a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion of silicon nitride over a first gate and a second portion of silicon nitride elevationally displaced from and in contact with the first portion, the first portion of silicon nitride having a greater stoichiometric amount of silicon than the second portion of silicon nitride and comprising Si_xN_y where a ratio of x to y is at least 1; and

a second gate over the silicon nitride layer.

49. (new) The gated semiconductor of claim 48 wherein the ratio of x to y is at least 1.75.

50. (new) The gated semiconductor of claim 48 wherein the ratio is 1, 1.75, or 10.

51. (new) The gated semiconductor of claim 48 wherein the second gate is a control gate of an EPROM or an EEPROM device.

52. (new) The gated semiconductor of claim 48 further comprising:

a silicon dioxide layer over said first portion; and

the second gate being over the silicon dioxide layer.

53. (new) A gated semiconductor assembly comprising:

a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion of silicon nitride over a floating gate and a second portion of silicon nitride elevationally displaced from and in contact with the first portion, the first portion of silicon nitride having a greater stoichiometric amount of silicon than the second portion of silicon nitride and a ratio of silicon to nitrogen exhibiting a refractive index of at least 2.2; and

a control gate over the silicon nitride layer.

54. (new) The gated semiconductor of claim 53 further comprising:

the second portion of the silicon nitride layer being over the first portion;

a silicon dioxide layer over said second portion; and

the control gate being over the silicon dioxide layer.

55. (new) The gated semiconductor of claim 53 wherein the refractive index is at least 2.5.

56. (new) The gated semiconductor of claim 53 wherein the ratio is 1, 1.75, or 10.

57. (new) A gated semiconductor assembly comprising:

a substrate;

a polycrystalline silicon layer over the substrate;

a silicon nitride layer over the polycrystalline silicon layer, the silicon nitride layer comprising a first portion of silicon nitride and a second portion of silicon nitride elevationally displaced from and in contact with the first portion, the first portion of silicon nitride having a greater stoichiometric amount of silicon than the second portion of silicon nitride and comprising Si_xN_y where a ratio of x to y is at least 1.75; and

a control gate over the silicon nitride layer.

58. (new) The gated semiconductor of claim 57 wherein the first portion is over the second portion.

59. (new) The gated semiconductor of claim 57 wherein the control gate is a control gate of an EPROM or an EEPROM device.

60. (new) The gated semiconductor of claim 57 wherein the second portion is over the first portion.

61. (new) The gated semiconductor of claim 57 further comprising:

a silicon dioxide layer over said first portion; and

the control gate being over the silicon dioxide layer.

62. (new) The gated semiconductor of claim 57 wherein the first portion exhibits a refractive index of at least 2.5.

63. (new) The gated semiconductor of claim 57 wherein the ratio is 1, 1.75, or 10.

64. (new) A gated semiconductor assembly comprising:

a substrate;

a floating gate over the substrate;

a control gate over the floating gate; and

an electron barrier layer between the floating gate and the control gate, the electron barrier layer comprising a silicon nitride layer, the silicon nitride layer comprising a first portion of silicon nitride and a second portion of silicon nitride contacting the first portion, the second portion being elevationally displaced from the first portion, and the first portion of silicon nitride having a greater stoichiometric amount of silicon than the second portion of silicon nitride and comprising Si_xN_y where a ratio of x to y is at least 1.

65. (new) The gated semiconductor assembly of claim 64 wherein the first portion is over the second portion.

66. (new) The gated semiconductor assembly of claim 64 wherein the control gate is a control gate of an EPROM or an EEPROM device.

67. (new) The gated semiconductor assembly of claim 64 wherein the electron barrier layer further comprises a silicon dioxide layer disposed between the control gate and the silicon nitride layer.

68. (new) The gated semiconductor assembly of claim 64 wherein the floating gate comprises polycrystalline silicon and has at least one sidewall, and wherein the silicon nitride layer has at least one sidewall, the assembly further comprising a layer of silicon dioxide extending along said sidewalls of the silicon nitride layer and the polycrystalline silicon.

69. (new) A gated semiconductor assembly comprising:

a semiconductor substrate;

a silicon oxide layer disposed over the semiconductive substrate;

a floating gate disposed over the silicon oxide layer;

a silicon nitride-comprising layer disposed over the floating gate wherein the silicon nitride-comprising layer has a lower portion of silicon nitride and a upper portion of silicon nitride, the lower portion being in contact with the floating gate and having a first ratio of silicon to nitrogen of at least 1.75 and the upper portion being in contact with the lower portion and having a second ratio of silicon to nitrogen different from the first ratio; and

a control gate disposed over the silicon nitride-comprising layer.